FIG. 1

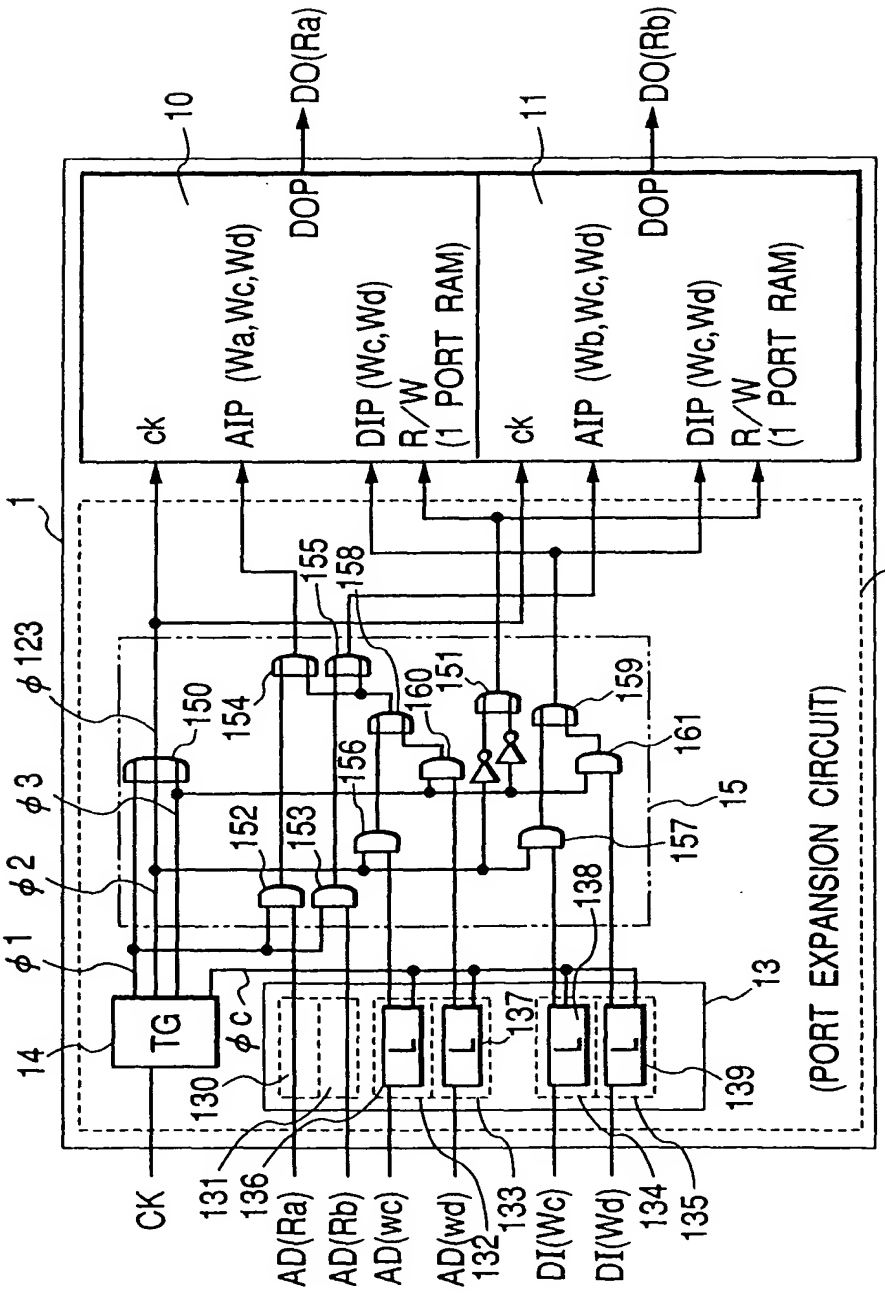

4 PORT RAM (USING TWO 1-PORT RAMS)
(PORT EXPANSION CIRCUIT)
10
11
12
13
14
15
ck
AIP (Wa,Wc,Wd)
DOP
DO(Ra)
DIP (Wc,Wd)
R/W
(1 PORT RAM)
AIP (Wb,Wc,Wd)
DO(Rb)
TG
L
CK
AD(Ra)
AD(Rb)
AD(wc)
AD(wd)
DI(Wc)
DI(Wd)
φ1
φ2
φ3
φ123
φc

FIG. 2

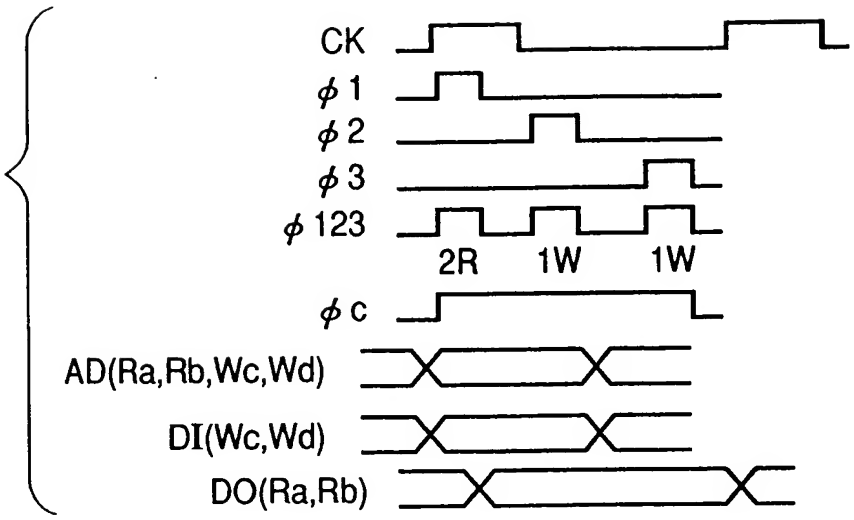

CK
φ1
φ2
φ3
φ123
2R 1W 1W
φc
AD(Ra,Rb,Wc,Wd)
DI(Wc,Wd)
DO(Ra,Rb)

FIG. 4

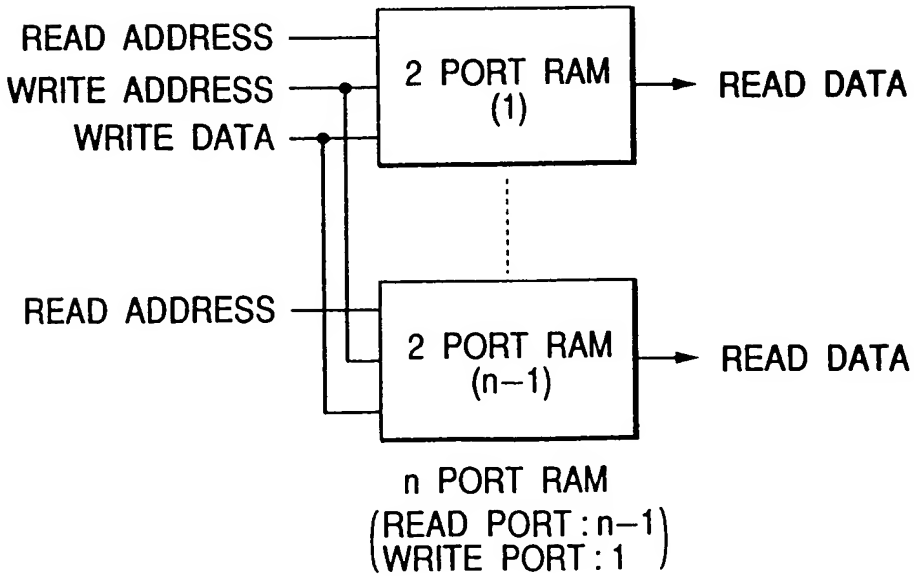

READ ADDRESS
WRITE ADDRESS
WRITE DATA
2 PORT RAM (1)
READ DATA
READ ADDRESS
2 PORT RAM (n−1)
READ DATA
n PORT RAM
(READ PORT : n−1
WRITE PORT : 1)

FIG. 3

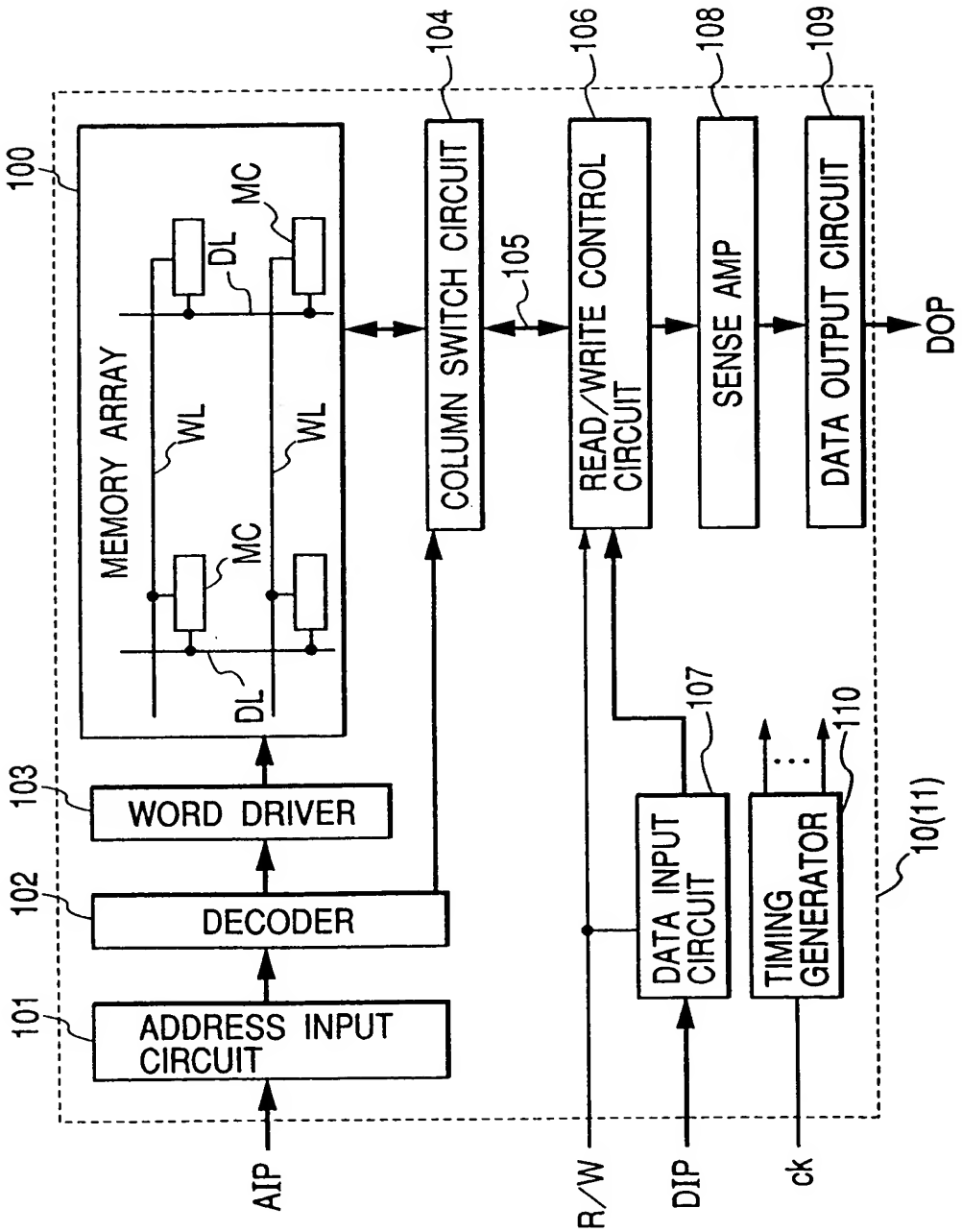

100
MEMORY ARRAY
WL
WL
DL
DL
MC
MC
101
ADDRESS INPUT CIRCUIT
102
DECODER
103
WORD DRIVER
104
COLUMN SWITCH CIRCUIT
105
106
READ/WRITE CONTROL CIRCUIT
107
108
SENSE AMP
109
DATA OUTPUT CIRCUIT
DOP
110
DATA INPUT CIRCUIT
TIMING GENERATOR
10(11)
AIP
R/W
DIP
ck

FIG. 5

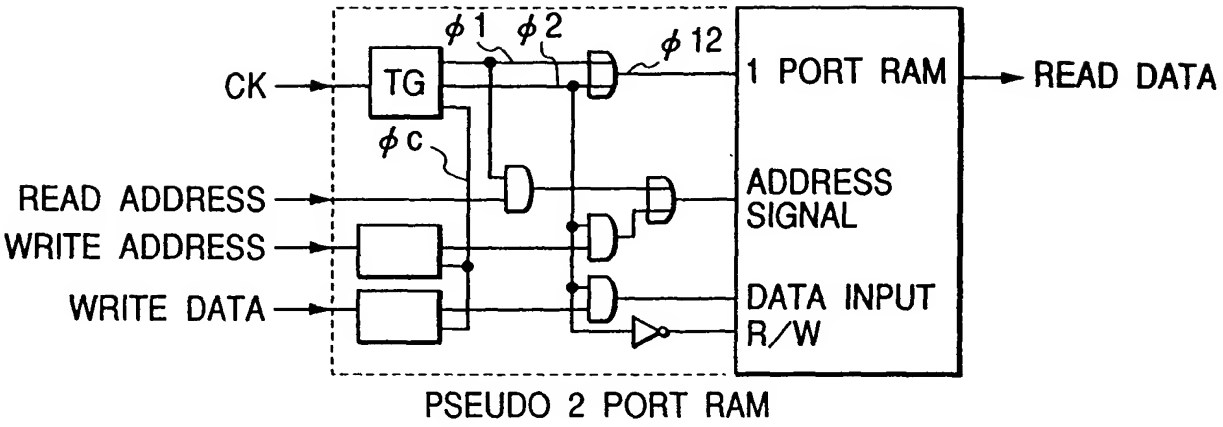

CK
TG
φ1
φ2
φ12
φc
READ ADDRESS
WRITE ADDRESS
WRITE DATA
1 PORT RAM
READ DATA
ADDRESS SIGNAL
DATA INPUT R/W
PSEUDO 2 PORT RAM

FIG. 6

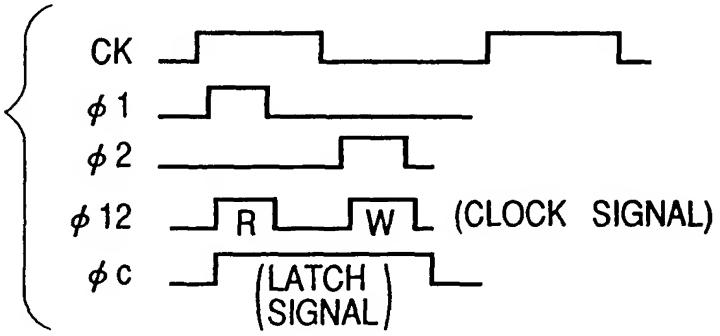
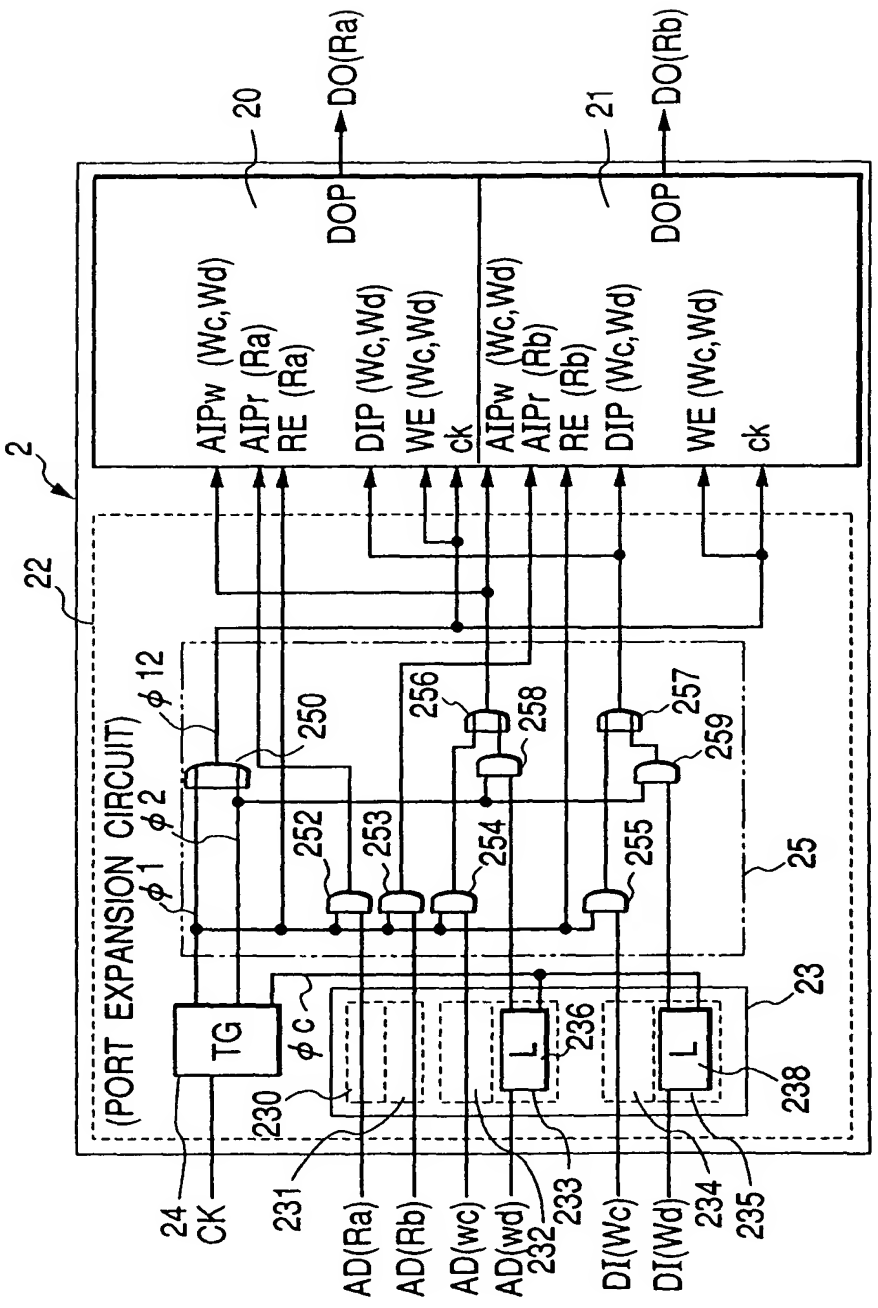

CK
φ1
φ2
φ12
R
W
(CLOCK SIGNAL)
φc
(LATCH SIGNAL)

FIG. 7



4 PORT RAM (USING TWO 2-PORT RAMS)

FIG. 8

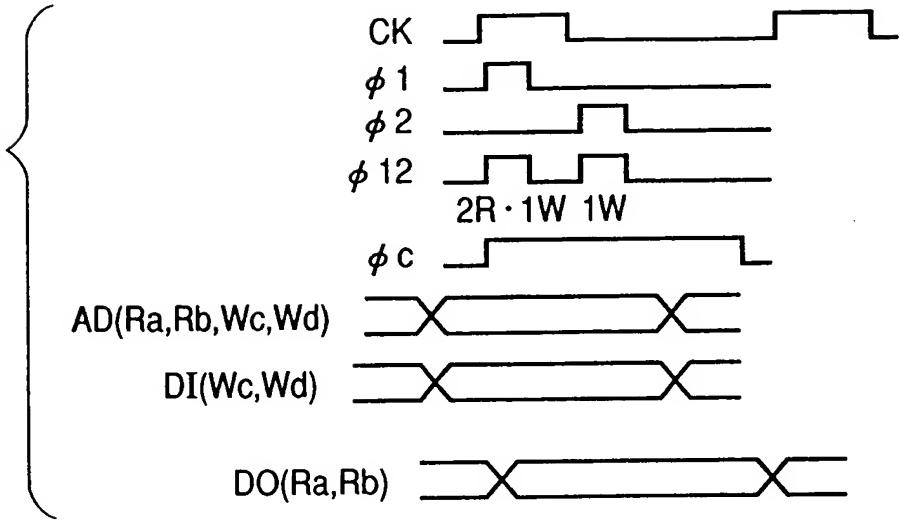

CK
φ1
φ2
φ12
2R・1W 1W
φc
AD(Ra,Rb,Wc,Wd)
DI(Wc,Wd)
DO(Ra,Rb)

FIG. 9

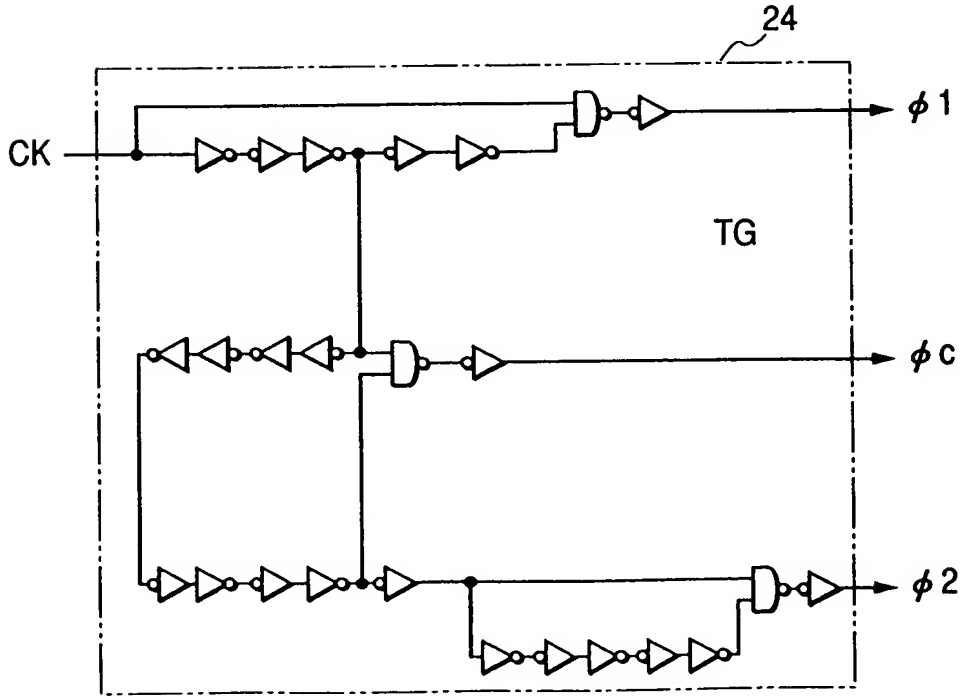

24
CK
φ1
TG
φc
φ2

FIG. 10

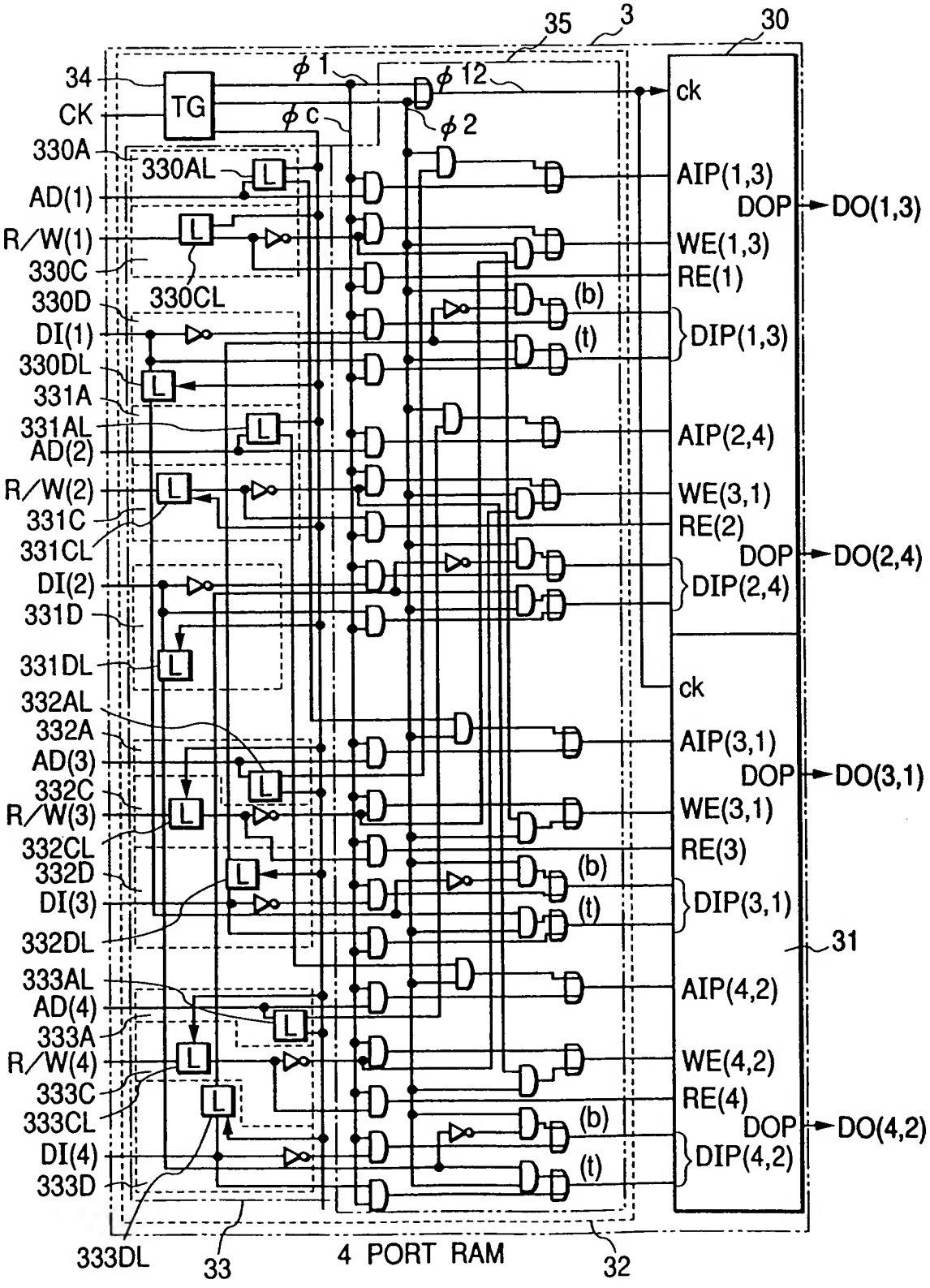

35
3
30
34
CK
TG
φ1
φc
φ12
φ2
ck
330A
330AL
AD(1)
AIP(1,3)
DOP
DO(1,3)
R/W(1)
WE(1,3)
330C
RE(1)
330D
330CL
(b)
DI(1)
(t)
DIP(1,3)
330DL
331A
331AL
AIP(2,4)
AD(2)
R/W(2)
WE(3,1)
331C
RE(2)
331CL
DOP
DO(2,4)
DI(2)
DIP(2,4)
331D
331DL
ck
332AL
AIP(3,1)
332A
AD(3)
DOP
DO(3,1)
332C
R/W(3)
WE(3,1)
332CL
RE(3)
332D
(b)
DI(3)
(t)
DIP(3,1)
332DL
31
333AL
AIP(4,2)
AD(4)
333A
R/W(4)
WE(4,2)
333C
RE(4)
333CL
(b)
DOP
DO(4,2)
DI(4)
(t)
DIP(4,2)
333D
333DL
33
4 PORT RAM
32

FIG. 11

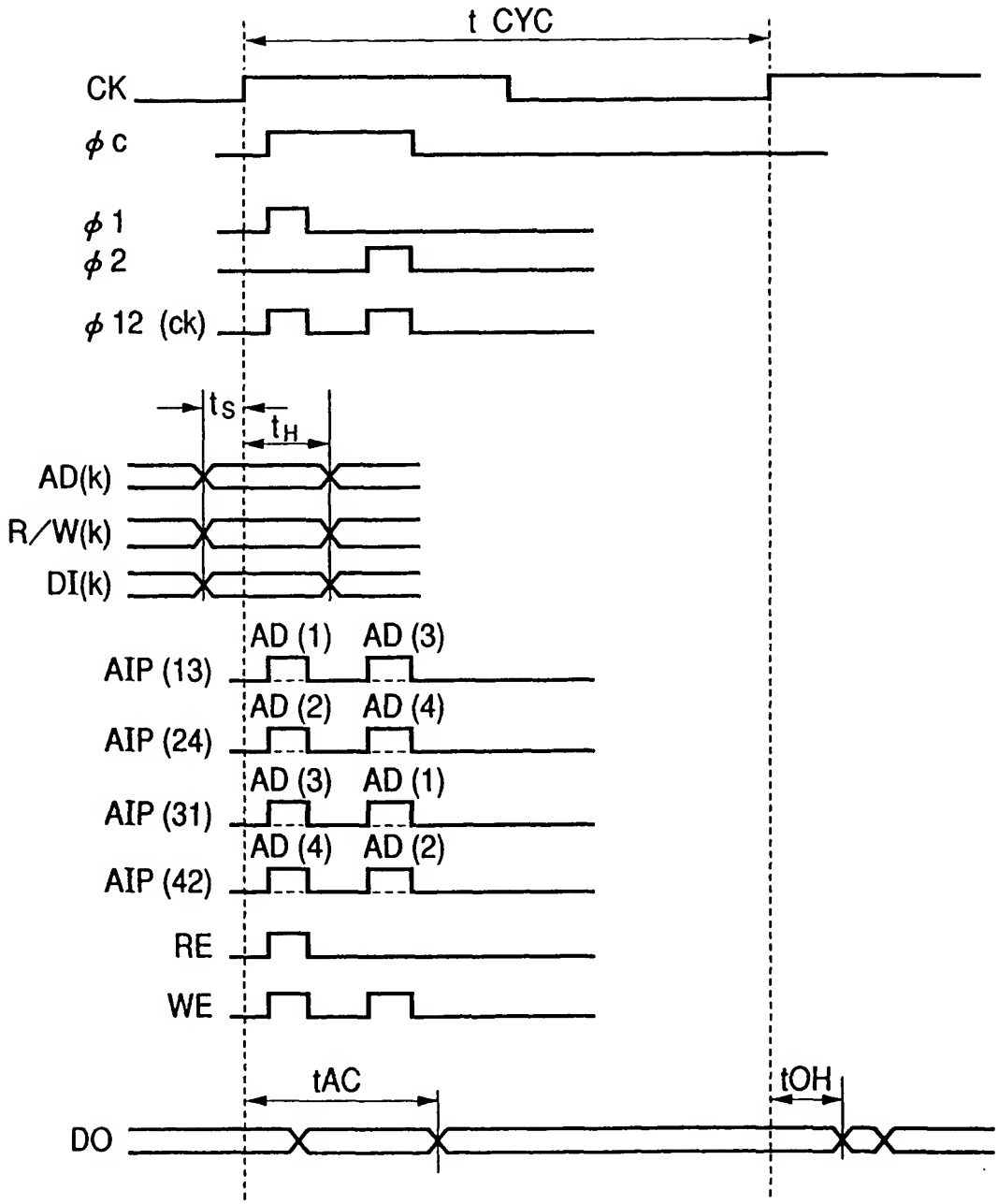

t CYC
CK
φc
φ1
φ2
φ12 (ck)
ts
tH
AD(k)
R/W(k)
DI(k)
AD (1) AD (3)
AIP (13)
AD (2) AD (4)
AIP (24)
AD (3) AD (1)
AIP (31)
AD (4) AD (2)
AIP (42)
RE
WE
tAC
tOH
DO

FIG. 12

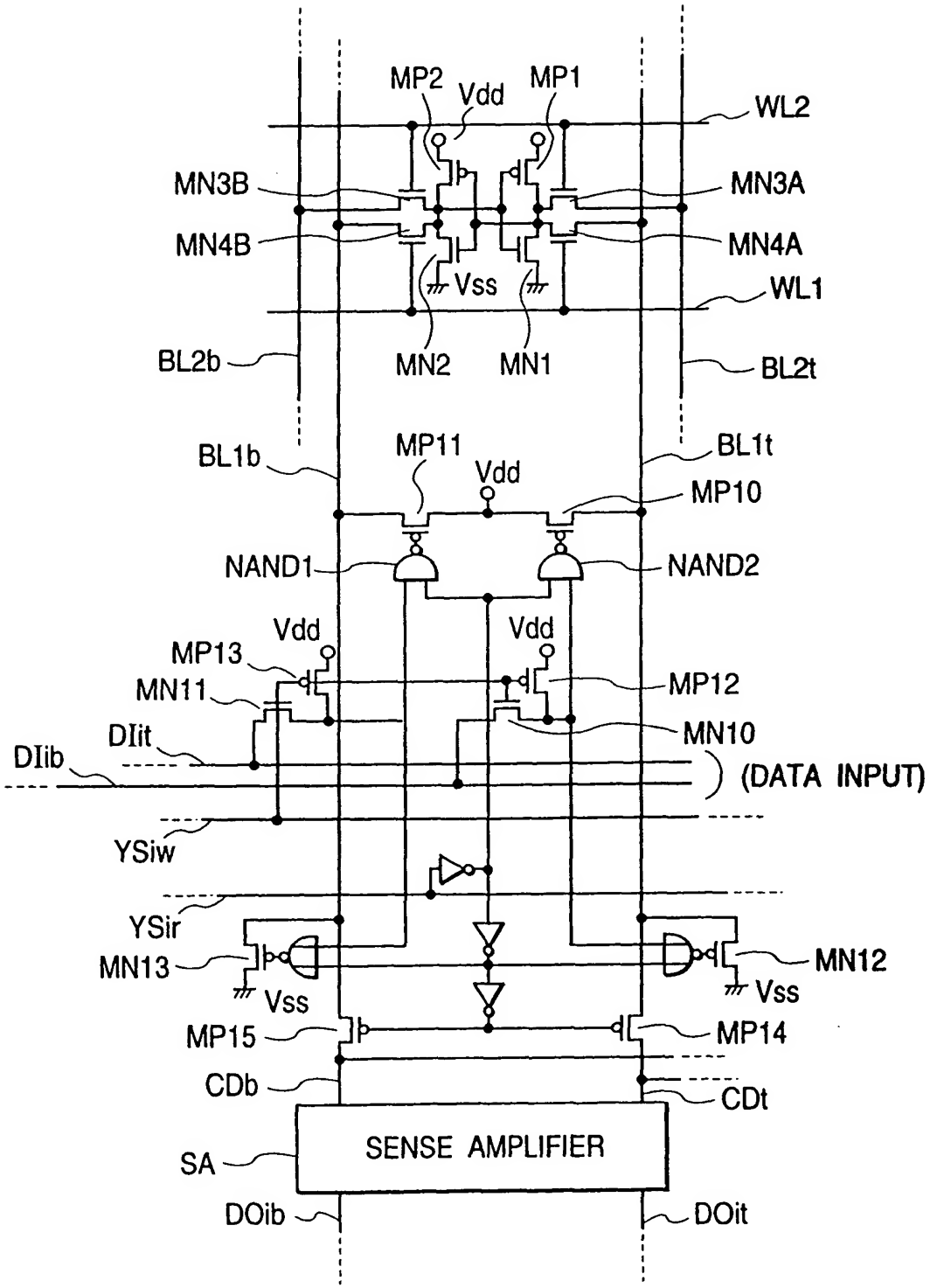

MP2
Vdd
MP1
WL2
MN3B
MN3A
MN4B
MN4A
Vss
WL1
BL2b
MN2
MN1
BL2t
BL1b
MP11
Vdd
BL1t
MP10
NAND1
NAND2
Vdd
Vdd
MP13
MP12
MN11
MN10
DIit
DIib
(DATA INPUT)
YSiw
YSir
MN13
MN12
Vss
Vss
MP15
MP14
CDb
CDt
SENSE AMPLIFIER
SA
DOib
DOit

FIG. 13

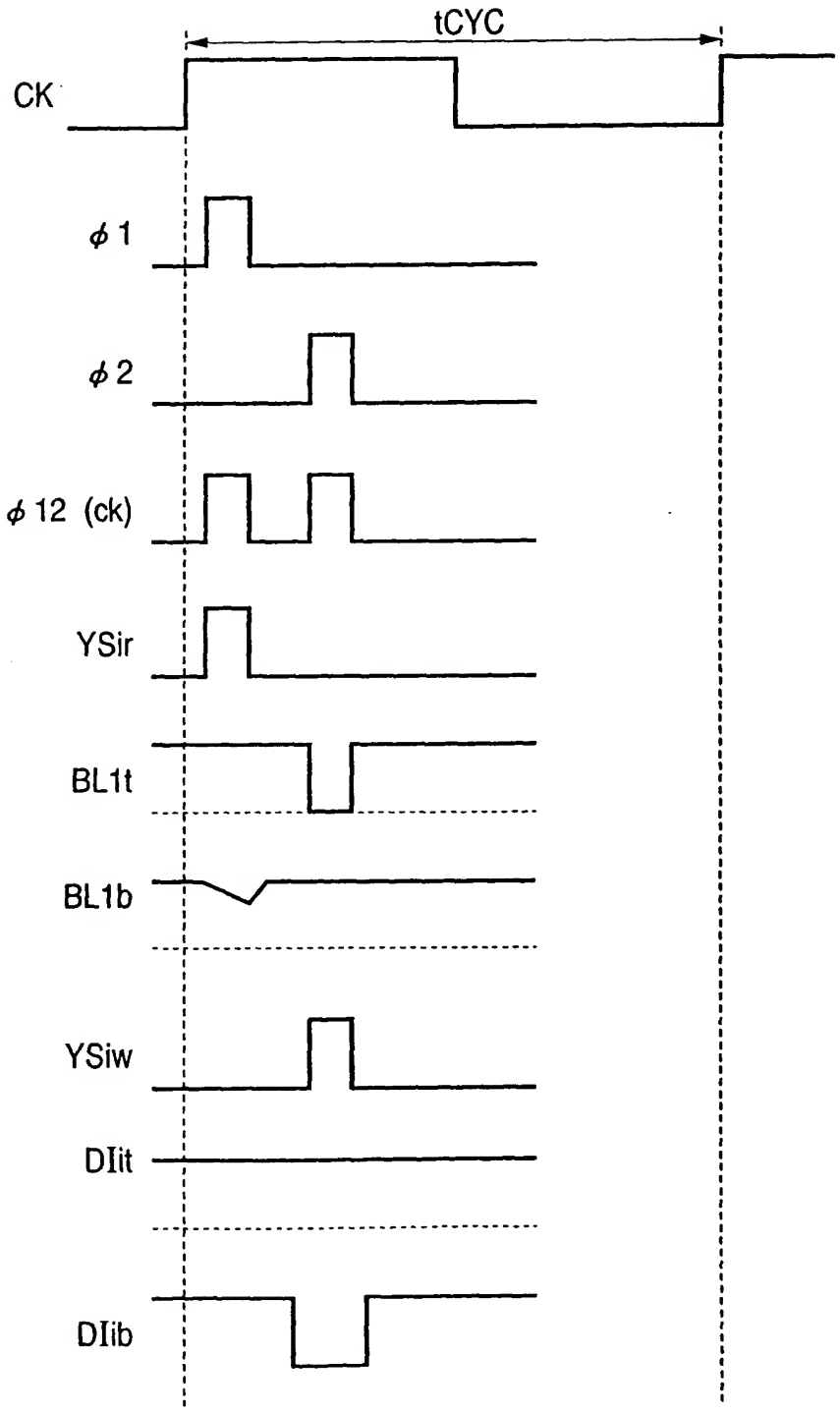
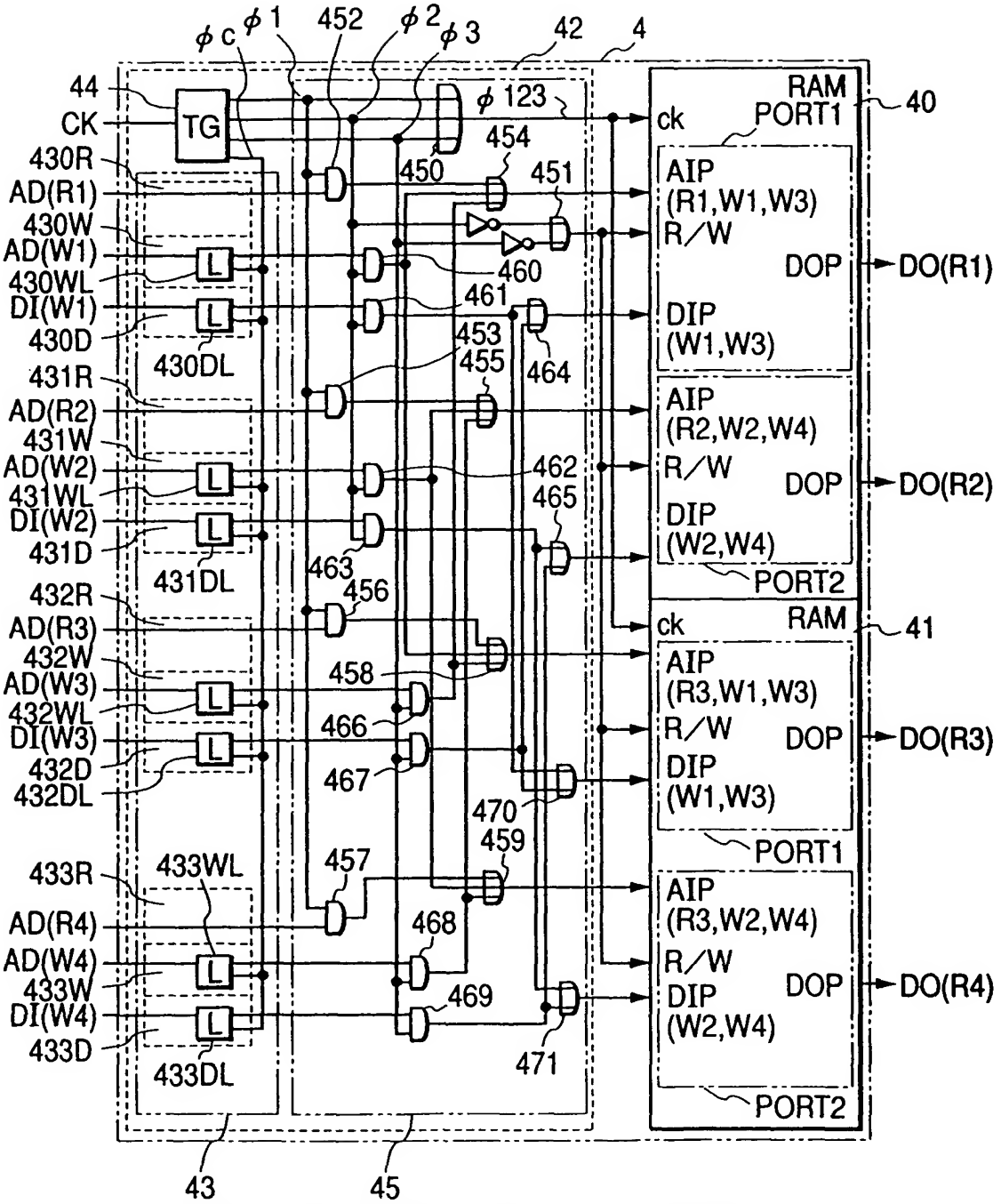


FIG. 14



8 PORT RAM (USING TWO 2-PORT RAMS)

FIG. 15

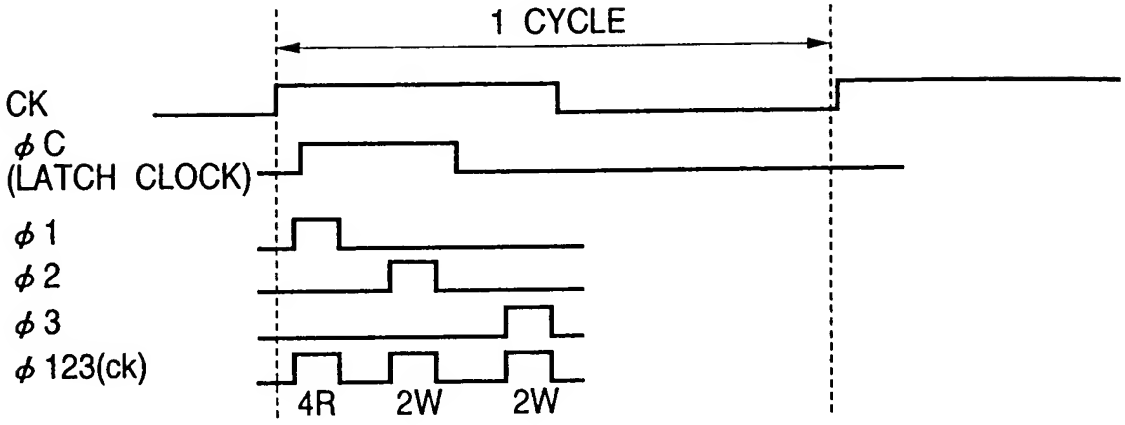


FIG. 16

INTERNAL RAM		FIRST (φ 1)	SECOND (φ 2)	THIRD (φ 3)
RAM 40	PORT1	AD (R1) DO (R1)	AD (W1) DI (W1)	AD (W3) DI (W3)
	PORT2	AD (R2) DO (R2)	AD (W2) DI (W2)	AD (W4) DI (W4)
RAM 41	PORT1	AD (R3) DO (R3)	AD (W1) DI (W1)	AD (W3) DI (W3)
	PORT2	AD (R4) DO (R4)	AD (W2) DI (W2)	AD (W4) DI (W4)

FIG. 17

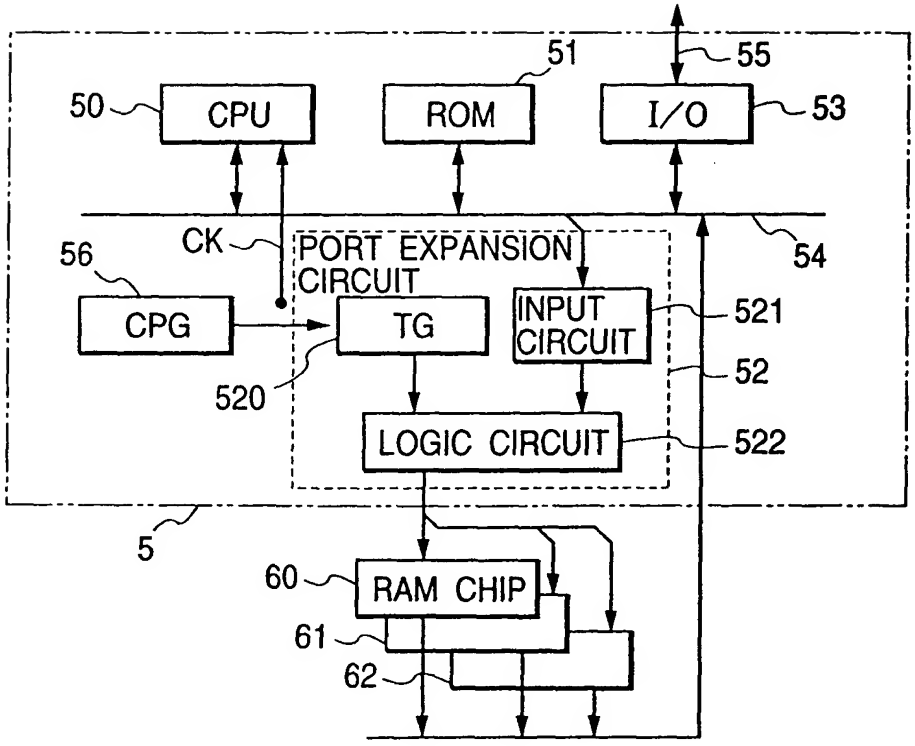
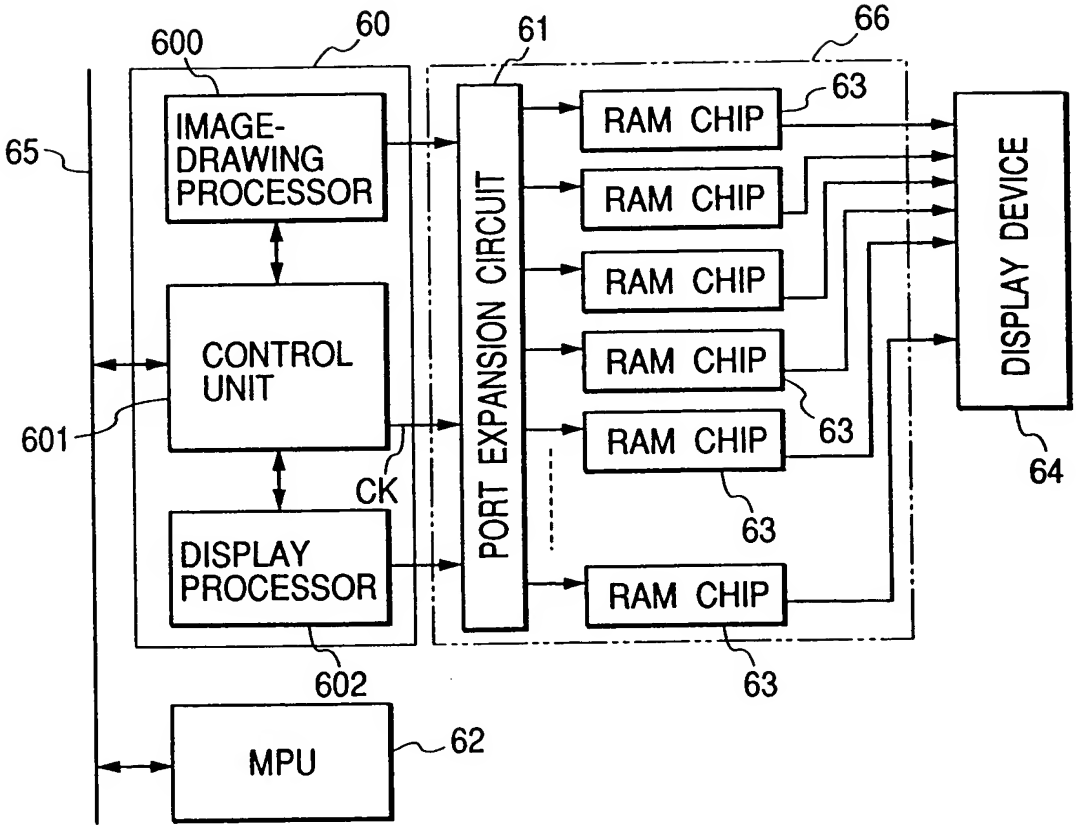

51
55
50
CPU
ROM
I/O
53
CK
PORT EXPANSION CIRCUIT
54
56
CPG
TG
INPUT CIRCUIT
521
520
52
LOGIC CIRCUIT
522
5
60
RAM CHIP
61
62

FIG. 18


600
60
61
66
63
65
IMAGE-DRAWING PROCESSOR
RAM CHIP
RAM CHIP
RAM CHIP
RAM CHIP
RAM CHIP
RAM CHIP
DISPLAY DEVICE
CONTROL UNIT
601
CK
PORT EXPANSION CIRCUIT
63
64
DISPLAY PROCESSOR
602
63
MPU
62